REMARKS

The Examiner rejected claims 1-30 under 35 U.S.C. §103(a) as allegedly being unpatentable over Lin (6,180,426 of record) in view of Arledge *et al.* (6,493,198).

Applicants respectfully traverse the §103 rejections with the following arguments.

35 USC § 103 Rejections

As to claim 1-33, the Examiner states that "Lin discloses a dual chip stack mounted on a module 320 (see figure 3), comprising: a semiconductor chip (310) including an integrated circuit having at least one first electrostatic discharge sensitive device (e.g., a transistor, Col 8-9); a non-semiconductor chip (305), attached to the semiconductor chip (310), the non-semiconductor chip (305) having at least one second electrostatic discharge sensitive device (e.g., a transistor, Col 8-9) and at least one fast electrostatic discharge protection device (e g., 414/418 in figures 4a-4b) electrically connected to the first electrostatic discharge sensitive device (via conductive bumps 3841315/394, see figure 3). Lm father teaches a second electrostatic protection device electrically connected to the second electrostatic discharge sensitive device (Col. 6, lines 9-67 and Col, 7, lines 1-67, Col, 89), Lim however, does not explicitly teach the electrostatic Protection device (ESD) being a spark gap having a substrate formed of an electrically insulating material. A spark gap, as disclosed by Arledge et al. (figures 1-3), being formed on a dielectric substrate (20) (Col. 2, lines 31-67), however, is commonly used in semiconductor art, as an electrostatic protection device (ESD), (see Arledge et al.' Col. 2-3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the spark gap as an electrostatic protection device (ESD) in Lin's device since such spark gap is conventionally used in semiconductor art as an electrostatic protection device (EST, as taught by Arledge et al."

Applicants contend that claim 1 is not obvious in view of Lin in view of Arledge because Lin in view of Arledge does not teach or suggest every feature of claim 1. For example, Lin in view of Arledge does not teach or suggest "a non-semiconductor chip." Applicants respectfully point out that both chips 305 and 310 of Lin are semiconductor chips.

First, Lin in col. 3, lines 38-42 states "The first integrated circuit chip could be fabricated using a first type of semiconductor process and the second integrated circuit chip would be fabricated with a second type of semiconductor process that is not compatible with the first type of semiconductor process."

Second, Lin's claim 1, states in part, "simultaneously but separately forming internal circuits on a first semiconductor wafer containing plural first integrated circuit chips and a second semiconductor wafer containing plural second integrated circuit chips."

Third, Lin, in col. 4, lines 11-19 most clearly indicates chips 305 and 310 are both integrated circuit chips by stating in part: "A first integrated circuit chip 305 is attached to a second integrated circuit chip 310." Integrated circuit chips are universally known to be semiconductor chips.

Fourth, Lin FIG. 3 clearly shows that chip 305 and includes the following identical components as chip 310: internal circuits 335 and 365 respectively, test interfaces 350 and 375 respectively, interchip interfaces 340 and 360 respectively. These components must be formed on semiconductor substrates. Therefore both chips 305 and 310 must be semiconductor chips.

Fifth, the circuits of FIGs. 4A and 4C of chip 305 are identical to respective circuits of FIGs 4B and 4D of chip 310 and both contain mode switches illustrated in Lin FIG. 5A and described in col. 8. The Examiner admits that Lin cols. 8-9 describe ESD sensitive transistors. The only elements specifically described as transistors are "n-channel metal-oxide semiconductor (NMOS) transistors 502a" and p-channel metal-oxide semiconductor (PMOS) transistors 502b" (col 8, lines 18-20) which must be formed in semiconductor substrates. Therefore, both chips 305 and 310 must be semiconductor chips.

Since claims 2 and 3 depend from claim 1, Applicants respectfully maintain that claims 2 and 3 are likewise in condition for allowance.

Applicants maintain that the arguments presented *supra* relative to claim 1 are applicable to claims 4, 8, 12, 15, 19, 23 and 26. Since claims 5-7 depend from claim 4, claims 9-11 depend from claim 8, Applicants maintain claims 5-7 and 9-11 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456

Respectfully submitted,
FOR: Malinowski et al.

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BY:
Jack P. Friedman
Reg. No. 44,688
FOR:
Anthony M. Palagonia
Registration No.: 41,237

3 Lear Jet Lane, Suite 201
Schmeiser, Olsen & Watts
Latham, New York 12110
(518) 220-1850
Agent Direct Dial Number: (802)-899-5460